MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
Sponsored by CMR Educational Society
(Affiliated to JNTU, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2008 Certified)
Maisammaguda, Dhulapally (Post Via Hakimpet), Secunderabad – 500100, Telangana State, India.
Contact Number: 040-23792146/64634237, E-Mail ID: mrcet2004@gmail.com, website: www.mrcet.ac.in

MASTER OF TECHNOLOGY
VLSI & EMBEDDED SYSTEMS

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC REGULATIONS
COURSE STRUCTURE AND SYLLABUS
(Batches admitted from the academic year 2015 - 2016)

Note: The regulations hereunder are subject to amendments as may be made by the Academic Council of the College from time to time. Any or all such amendments will be effective from such date and to such batches of candidates (including those already pursuing the program) as may be decided by the Academic Council.

PRELIMINARY DEFINITIONS AND NOMENCLATURES

*"Autonomous Institution /College" means an institution/college designated as autonomous institute / college by University Grants Commission (UGC), as per the UGC Autonomous College Statutes.

*"Academic Autonomy" means freedom to a College in all aspects of conducting its academic programs, granted by the University for promoting excellence.

*"Commission" means University Grants Commission.

*"AICTE" means All India Council for Technical Education.

*"University" the Jawaharlal Nehru Technological University, Hyderabad.

*"College" means Malla Reddy College of Engineering & Technology, Secunderabad unless indicated otherwise by the context.

*"Program" means:

Master of Technology (M.Tech) degree program

PG Degree Program: M.Tech

*"Branch" means specialization in a program like M.Tech degree program in Electronics and Communication Engineering, M.Tech degree program in Computer Science and Engineering etc.

*"Course" or "Subject" means a theory or practical subject, identified by its course – number and course-title, which is normally studied in a semester.

*T–Tutorial, P–Practical, D–Drawing, L-Theory, C-Credits

FOREWORD

The autonomy is conferred on Malla Reddy College of Engineering & Technology (MRCET) by UGC based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies like UGC and AICTE. It reflects the confidence of the UGC in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards degrees on behalf of the college. Thus, an autonomous institution is given the freedom to have its own curriculum, examination system and monitoring mechanism, independent of the affiliating University but under its observance.

Malla Reddy College of Engineering & Technology (MRCET) is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, and also improving upon the values and beliefs for which it has been striving for more than a decade in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Boards of Studies are constituted with the guidance of the Governing Body of the College and recommendations of the JNTU Hyderabad to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after prolonged and detailed interaction with several experts drawn from academics, industry and research, in accordance with the vision and mission of the college which reflects the mindset of the institution in order to produce quality engineering graduates to the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications, if needed, are to be sought at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The Cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the institution and brighter prospects of engineering graduates.

"A thought beyond the horizons of success committed for educational excellence"

PRINCIPAL

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)
Sponsored by CMR Educational Society
(Affiliated to JNTU, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2008 Certified)
Maisammaguda, Dhulapally (Post Via Hakimpet), Secunderabad – 500100, Telangana State, India.
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VISION

- To establish a pedestal for the integral innovation, team spirit, originality and competence in the students, expose them to face the global challenges and become technology leaders of Indian vision of modern society.

MISSION

- To become a model institution in the fields of Engineering, Technology and Management.
- To impart holistic education to the students to render them as industry ready engineers.
- To ensure synchronization of MRCET ideologies with challenging demands of International Pioneering Organizations.

QUALITY POLICY

- To implement best practices in Teaching and Learning process for both UG and PG courses meticulously.
- To provide state of art infrastructure and expertise to impart the quality education.
- To groom the students to become intellectually creative and professionally competitive.
- To channelize the activities and tune them in heights of commitment and sincerity, the requisites to claim the never ending ladder of SUCCESS year after year.

For more information: www.mrcet.ac.in

ACADEMIC REGULATIONS R-15 FOR M. TECH. (REGULAR) DEGREE COURSE

Academic Regulations of R-15 are applicable for the students of M. Tech. (Regular) Course from the Academic Year 2015-16 and onwards. The M.Tech Degree of Malla Reddy College of Engineering & Technology (MRCET), Secunderabad shall be conferred on candidates who are admitted to the program and who fulfill all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University (or) State Government (or) on the basis of any other order of merit as approved by the University, subject to norms as laid down by the State Govt. from time to time.

2.0 AWARD OF M. TECH. DEGREE

2.1. A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years.
2.2. A student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his admission, shall forfeit his seat in M. Tech. course.
2.3. The student shall register for all 88 credits and secure all the 88 credits.
2.4. The minimum instruction days in each semester are 90.

3.0 A. COURSE OF STUDY

The following specializations are offered at present for the M. Tech. course of study.

1. Aerospace Engineering
2. Computer Science and Engineering
3. Machine Design
4. System and Signal Processing
5. VLSI and Embedded Systems
6. Thermal Engineering

and any other course as approved by the MRCET from time to time.

3.0 B. Departments offering M. Tech. Programmes with specializations are noted below:

Aeronautical Engineering	Aerospace Engineering
Computer Science Engineering	Computer Science Engineering
Electronics & Communication Engineering	System & Signal Processing
Electronics & Communication Engineering	VLSI and Embedded Systems
Mechanical Engineering	Machine Design
Mechanical Engineering	Thermal Engineering

4.0 ATTENDANCE

The programs are offered on a unit basis with each subject being considered a unit.

4.1 A student shall be eligible to write University examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

4.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee.

4.3 Shortage of Attendance below 65% in aggregate shall not be condoned.

4.4 Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of that class and their registration shall stand cancelled.

4.5 A prescribed fee as determined by the examination branch shall be payable towards condonation of shortage of attendance.

4.6 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

4.7 In order to qualify for the award of the M. Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

4.8 A student shall not be promoted to the next semester unless he satisfies the minimum academic requirements of the previous semester.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

For the theory subjects 75 marks shall be awarded based on the performance in the End Semester Examination and 25 marks shall be awarded based on the Internal Examination Evaluation. The internal evaluation consists of two mid-term examination of 25 marks each covering descriptive paper which consists 5 questions consisting of two parts each (a) and (b), out of which the student has to answer either (a) or (b), not both. Each question carries 5 marks for a total duration of 2 hours. The total marks secured by the student in each mid-term examination are evaluated for 25 marks, and the average of the two mid-term examinations shall be taken as the final marks secured by each candidate.

However, any student scoring internal marks less than 40% will be given a chance to write the internal exam once again after he/she re-registering for the concerned subject and paying stipulated fees as per the norms.

5.1 The end semesters examination will be conducted for 75 marks with 5 questions consisting of two questions each (a) and (b), out of which the student has to answer

either (a) or (b), not both and each question carries 15 marks.

5.2 For practical subjects, 75 marks shall be awarded based on the performance in the End Semester Examinations and 25 marks shall be awarded based on the day-to-day performance as Internal Marks.

5.3 There shall be two seminar presentations during I year I semester and II semester respectively. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Examination taken together.

5.5 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.4) he has to reappear for the End semester Examination in that subject.

5.6 A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and so has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled.

5.7 In case the candidate secures less than the required attendance in any subject, he shall not be permitted to write the End Examination in that subject. He shall re-register the subject when next offered.

5.8 Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher and the second examiner shall be another Laboratory Teacher.

6.0 EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

6.1 A Project Review Committee (PRC) shall be constituted with Principal as Chairperson, Heads of all the Departments offering the M. Tech. programs and two other senior faculty members.

6.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the Departmental Academic Committee for approval. Only after obtaining the approval of the Departmental Academic Committee can the student initiate the

Project work.

6.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Departmental Academic Committee. However, the Departmental Academic Committee shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.5 A candidate shall submit his status report in a bound-form in two stages at least with a gap of 3 months between them.

6.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal through Head of the Department and make an oral presentation before the PRC.

6.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/School/Institute.

6.8 The thesis shall be adjudicated by one examiner selected by the University. For this, the Principal of the College shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned and head of the department.

6.9 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

6.10 If the report of the examiner is favorable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report the candidate's work as one of the following:

A. Excellent
B. Good
C. Satisfactory
D. Unsatisfactory

The Head of the Department shall coordinate and make arrangements for the conduct of Viva- Voce examination.

If the report of the Viva-Voce is unsatisfactory, the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva- Voce examination, he will not be eligible for the award of the degree.

7.0 AWARD OF DEGREE AND CLASS

In assessing the performance of the students in examinations, the usual approach is to award marks based on the examinations conducted at various stages (sessional, mid-term, end-semester etc.,) in a semester. As per UGC Autonomous guidelines, the following system is implemented in awarding the grades and CGPA under the Credit Based Semester System (CBCS).

Letter Grades and Grade Points:
The UGC recommends a 10-point grading system with the following letter grades as given below:

Grades	Points	Marks secured (%)
O (Outstanding)	10	≥ 85
A+(Excellent)	9	80 – 84
A(Very Good)	8	75 – 79
B+(Good)	7	70 – 74
B(Above Average)	6	65 – 69
C(Average)	5	60 – 64
P(Pass)	4	50 – 59
F(Fail)	0	<50
Ab(Absent)	0	-

A student obtaining Grade F shall be considered failed and will be required to reappear in the examination

Computation of SGPA and CGPA

The UGC recommends the following procedure to compute the Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

i. The SGPA is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e

SGPA (S_i) = $\Sigma(C_i \times G_i) / \Sigma C_i$

where C_i is the number of credits of the i^{th} course and G_i is the grade point scored by the student in the i^{th} course.

ii. The CGPA is also calculated in the same manner taking into account all the courses undergone by a student over all the semesters of a programme, i.e.

CGPA = $\Sigma(C_i \times S_i) / \Sigma C_i$

where S_i is the SGPA of the i^{th} semester and C_i is the total number of credits in that semester.

iii. The SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

8.0 WITHHOLDING OF RESULTS

If the student has not paid the dues, if any, to the Institute or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be withheld in such cases.

9.0 TRANSITORY REGULATIONS

9.1 Discontinued, detained, or failed candidates are eligible for admission to two earlier or equivalent subjects at a time as and when offered.

10. GENERAL

10.1 Wherever the words he, him, his, occur in the regulations, they include she, her, hers .

10.2 The academic regulation should be read as a whole for the purpose of any interpretation.

10.3 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council of the College is final.

10.4 The College may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Academic Council of the College/Affiliating University.

MALPRACTICES RULES
DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

S.No	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals

		and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the othe subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Using objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for

	person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-incharge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	the remaining examinations of the subjects of that semester. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other

	clause 6 to 8.	subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Academic Council of the College (or) affiliating University for further action towards suitable punishment.	

Malpractices identified by squad or special invigilators will entail punishment to the candidates as per the above guidelines..

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
M.TECH – VLSI & EMBEDDED SYSTEMS
COURSE STRUCTURE

I Year I Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/ P/ D	C	MAX MARKS	
						INT	EXT
1	R15D6801	VLSI Technology & Design	4	-	3	25	75
2	R15D6802	CPLD & FPGA Architectures & Applications	4	-	3	25	75
3	R15D6803	Embedded System design	4	-	3	25	75
4	R15D6804 R15D6805 R15D6806	ELECTIVE-I 1.Digital System Design 2.CMOS Analog Integrated Circuit Design 3.Hardware Software Co-design	4	-	3	25	75
5	R15D6807 R15D6808 R15D6809	ELECTIVE-II 1.CMOS Digital Integrated Circuit design 2.Algorithms for VLSI Design Automation 3.Advanced Digital Signal Processing	4	-	3	25	75
6	R15D5802 R15D5803 R15D5812	OPEN ELECTIVE –I 1.Advanced Operating Systems 2.Computer System Design 3.Web Services and Service oriented Architecture	4	-	3	25	75
7	R15D6881	VLSI Laboratory	-	3	2	25	75
8	R15D6882	Technical Seminar-I	-	-	2	50	-
Total			24	3	22	225	525

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

I Year II Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R15D6810	Embedded Real Time Operating Systems	4	-	3	25	75
2	R15D6811	CMOS Mixed Signal Circuit Design	4	-	3	25	75
3	R15D6812	Low Power VLSI Design	4	-	3	25	75
4	R15D6813 R15D6814 R15D6815	ELECTIVE – III 1.Adhoc –Wireless Networks 2.Digital Signal Processors & Architectures 3.Embedded Networking	4	-	3	25	75
5	R15D6816 R15D6817 R15D6818	ELECTIVE- IV 1.System On Chip Architecture 2.Design For Testability 3.Multimedia Signal Coding	4	-	3	25	75
6	R15D5805 R15D5810 R15D5816	OPEN ELECTIVE- II 1.Natural Language Processing 2.Advanced Network Programming 3.Grid and Cloud Computing	4	-	3	25	75
7	R15D6883	Embedded Systems Laboratory	-	3	2	25	75
8	R15D6884	Technical Seminar-II	-	-	2	50	-
Total			24	3	22	225	525

II Year I Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	-	Project Review Seminars	-	-	4	-	-
2	-	Project Work	-	-	18	-	-
Total			-	-	22	-	-

II Year II Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	-	Project Work	-	-	22	-	-
2	-	Project Viva-voce	-	-	-	-	-
Total			-	-	22	-	-

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(AUTONOMOUS)
M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

VLSI TECHNOLOGY AND DESIGN

UNIT –I:

Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: I_{ds} – V_{ds} relationships, Threshold Voltage V T , G m , G ds and ω o , Pass ransistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu} /Z_{pd} , MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:

Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:

Combinational Logic Networks:

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks,Gate and Network testing.

UNIT –IV:

Sequential Systems:

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V:

Floor Planning:

Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3 rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2 nd Ed., Addison Wesley.

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

UNIT-I:

Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation

UNIT-II:

Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures,Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV:

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:

Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

EMBEDDED SYSTEM DESIGN

UNIT –I:

ARM Architecture:

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:

ARM Programming Model – I:

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions,

PSR Instructions, Conditional Instructions.

UNIT –III:

ARM Programming Model – II:

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:

ARM Programming:

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:

Memory Management:

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.
2. Professional Embedded ARM development-James A Langbridge, Wiley/Wrox

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.
2.ARM System on Chip Architecture, Steve Furber, 2nd Edition, Pearson

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EMBEDDED SYSTEM DESIGN

UNIT –I:

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UNIT –II:

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Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions,PSR Instructions, Conditional Instructions.

UNIT –III:

ARM Programming Model – II:

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:

ARM Programming:

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic,Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:

Memory Management:

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

2. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

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DIGITAL SYSTEM DESIGN
(ELECTIVE -I)

UNIT -I:

Minimization and Transformation of Sequential Machines:

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II:

Digital Design:

Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III:

SM Charts:

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:

Fault Modeling & Test Pattern Generation:

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques,Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:

Fault Diagnosis in Sequential Circuits:

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5 th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:

1. Switching and Finite Automata Theory – Z. Kohavi , 2 nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4 th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

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M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

CMOS ANALOG INTEGRATED CIRCUIT DESIGN
(ELECTIVE -I)

UNIT -I:

MOS Devices and Modeling:

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II:

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III:

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV:

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V:

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li

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M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

HARDWARE - SOFTWARE CO-DESIGN
(ELECTIVE -I)

UNIT –I:

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II:

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:

Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies,practical consideration in a compiler development environment.

UNIT –IV:

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.

2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

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CMOS DIGITAL INTEGRATED CIRCUIT DESIGN
(ELECTIVE – II)

UNIT –I:

MOS Design:

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage,Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates,Transistor equivalency, CMOS Inverter logic.

UNIT –II:

Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:

Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV:

Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:

Semiconductor Memories:

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3 rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2 nd Ed., PHI.

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M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

ALGORITHMS FOR VLSI DESIGN AUTOMATION
(ELECTIVE-II)

UNIT I

PRELIMINARIES

Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION

Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING

Problems, Concepts and Algorithms.

MODELLING AND SIMULATION

Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT III

LOGIC SYNTHESIS AND VERIFICATION

Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

HIGH-LEVEL SYNTHESIS

Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aqspects of Assignment problem, High-level Transformations.

UNIT IV

PHYSICAL DESIGN AUTOMATION OF FPGA'S

FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT V

PHYSICAL DESIGN AUTOMATION OF MCM'S

MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXT BOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.

2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rdEd., 2005, Springer International Edition.

REFERENCES:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.

2.Modern VLSI Design:S ystems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia

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ADVANCED DIGITAL SIGNAL PROCESSING
(ELECTIVE-II)

ADVANCED DIGITAL SIGNAL PROCESSING
(ELECTIVE-II)

UNIT I

Review of DFT, FFT, IIR Filters, FIR Filters,

Multirate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multirate Signal Processing

UNIT II

Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT III

Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT –IV

Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

UNIT V

Finite Word Length Effects: Analysis of finite word length effects in Fixed-point DSP systems – Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications - J.G.Proakis & D.G.Manolokis, 4th ed., PHI.
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
3. DSP – A Pratical Approach – Emmanuel C.Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

REFERENCES:

1. Modern spectral Estimation : Theory & Application – S. M .Kay, 1988, PHI.
2. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education

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M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

ADVANCED OPERATING SYSTEMS
(OPEN ELECTIVE-I)

UNIT I

Real-time operating systems: Design issues, principles and case study.

UNIT II

Distributed operating system: Design issues, features and principles of working, case study.

UNIT III

Network operating system: Design issues, working principles and characteristic features, case study.

UNIT IV

Kernel development: Issues and development principles, case study.

UNIT V

Protection, privacy, access control and security issues, solutions.

TEXT BOOKS:

1. A.Silberschatz - Applied Operating System Concepts, Wiley, 2000.
2. Lubemir F Bic and Alan C. Shaw - Operating System Principles, Pearson Education, 2003.

REFERENCE BOOKS:

1. Operating Systems : Internal and Design Principles - Stallings, 6th ed., PE.
2. Modern Operating Systems, Andrew S Tanenbaum 3rd ed., PE.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th ed.,, John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens ,1998, PHI.
6. The UNIX Programming Environment – Kernighan & Pike, PE.

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
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M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

COMPUTER SYSTEM DESIGN
(OPEN ELECTIVE-I)

UNIT I

Computer structure – hardware, software, system software, Von-Neumann architecture – case study. IA -32 Pentium: registers and addressing, instructions, assembly language, program flow control, logic and shift/rotate instructions, multiply, divide MMX, SIMD instructions, I/O operations, subroutines.

Input/output organization, interrupts, DMA, Buses, Interface circuits, I/O interfaces, device drivers in windows, interrupt handlers

UNIT II

Processing Unit: Execution of a complete instruction, multiple bus organization, hardwired control, micro programmed control.

Pipelining: data hazards, instruction hazards, influence on instruction sets, data path & control consideration, and RISC architecture introduction.

UNIT – III

Memory: types and hierarchy, model level organization, cache memory, performance considerations, mapping, virtual memory, swapping, paging, segmentation, replacement policies.

UNIT – IV

Processes and Threads: processes, threads, inter process communication, classical IPC problems, Deadlocks.

UNIT – V

File system: Files, directories, Implementation, Unix file system

Security: Threats, intruders, accident data loss, basics of cryptography, user authentication.

TEXT BOOKS:

1. Computer Organization – Car Hamacher, Zvonks Vranesic, SafeaZaky, Vth Edition, McGraw Hill.
2. Modern Operating Systems, Andrew S Tanenbaum 2nd edition Pearson/PHI

REFERENCE BOOKS:

1. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson /PHI
2. Morris Mano- Computer System Architecture –3rd Edition-Pearson Education.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne 7th Edition, John Wiley
4. Operating Systems – Internals and Design Principles Stallings, Fifth Edition–2005, Pearson Education/PHI

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M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

WEB SERVICES AND SERVICE ORIENTED ARCHITECTURE
(OPEN ELECTIVE-I)

UNIT I

Evolution and Emergence of Web Services – Evolution of distributed computing. Core distributed computing technologies – client/server, CORBA, JAVA RMI, Micro Soft DCOM, MOM, Challenges in Distributed Computing, role of J2EE and XML in distributed computing, emergence of Web Services and Service Oriented Architecture (SOA). Introduction to Web Services – The definition of web services, basic operational model of web services, tools and technologies enabling web services, benefits and challenges of using web services.

UNIT II

Web Service Architecture – Web services Architecture and its characteristics, core building blocks of web services, standards and technologies available for implementing web services, web services communication, basic steps of implementing web services. Describing Web Services – WSDL introduction, non functional service description, WSDL1.1 Vs WSDL 2.0, WSDL document, WSDL elements, WSDL binding, WSDL tools, WSDL port type, limitations of WSDL.

UNIT III

Brief Over View of XML – XML Document structure, XML namespaces, Defining structure in XML Documents, Reuse of XML schemes, Document navigation and transformation. SOAP : Simple Object Access Protocol, Inter-application communication and wire protocols, SOAP as a messaging protocol, Structure of a SOAP message, SOAP envelope, Encoding, Service Oriented Architectures, SOA revisited, Service roles in a SOA, Reliable messaging, The enterprise Service Bus, SOA Development Lifecycle, SOAP HTTP binding, SOAP communication model, Error handling in SOAP.

UNIT IV

Registering and Discovering Services : The role of service registries, Service discovery, Universal Description, Discovery, and Integration, UDDI Architecture, UDDI Data Model, Interfaces, UDDI Implementation, UDDI with WSDL, UDDI specification, Service Addressing and Notification, Referencing and addressing Web Services, Web Services Notification.

UNIT V

SOA and web services security considerations, Network-level security mechanisms, Application-level security topologies, XML security standards, Semantics and Web Services, The semantic interoperability problem, The role of metadata, Service metadata, Overview of .NET and J2EE, SOA and Web Service Management, Managing Distributed System, Enterprise management Framework, Standard distributed management frameworks, Web service management, Richer schema languages, WS-Metadata Exchange.

TEXT BOOKS:

1. Web Services & SOA Principles and Technology, Second Edition, Michael P. Papazoglou.
2. Developing Java Web Services, R. Nagappan, R. Skoczylas, R.P. Sriganesh, Wiley India.
3. Developing Enterprise Web Services, S. Chatterjee, J. Webber, Pearson Education.

REFERENCE BOOKS:

1. XML, Web Services, and the Data Revolution, F.P.Coyle, Pearson Education.
2. Building web Services with Java, 2nd Edition, S. Graham and others, Pearson Education.
3. Java Web Services, D.A. Chappell & T. Jewell, O'Reilly, SPD.
4. McGovern, et al., "Java web Services Architecture", Morgan Kaufmann Publishers, 2005.
5. J2EE Wer Services, Richard Monson-Haefel, Pearson Education.

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
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M. Tech – I Year – I Sem. (VLSI & Embedded Systems)

VLSI LABORATORY

Note:
Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.

Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:
Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
11. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, multiplication and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits

Part –II: VLSI Back End Design programs:

Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitic and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing Analysis, IR drops analysis and crosstalk analysis of the following:

- Basic logic gates
- CMOS inverter
- CMOS NOR/ NAND gates
- CMOS XOR and MUX gates
- CMOS 1-bit full adder
- Static / Dynamic logic circuit (register cell)
- Latch
- Pass transistor Basic logic gates

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths

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M. Tech – I Year – IISem. (VLSI & Embedded Systems)

EMBEDDED REAL TIME OPERATING SYSTEMS

UNIT – I:
Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read,write), Process Control (fork, vfork, exit, wait, waitpid, exec.

UNIT - II:
Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS,Defining a Task asks States and Scheduling, Task Operations, Structure, Synchronization,
Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:
Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:
Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V:
Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:
1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011
REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

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CMOS MIXED SIGNAL CIRCUIT DESIGN

UNIT -I:
Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing,biquad filters.

UNIT -II:
Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency
detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities,Jitter in PLLs, Delay locked loops, applications

UNIT -III:
Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:
Nyquist Rate A/D Converters:
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V:
Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press,International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:
1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche,Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

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M. Tech – I Year – IISem. (VLSI & Embedded Systems)

LOW POWER VLSI DESIGN

UNIT –I:

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation,Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, ShortChannel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, VelocitySaturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques–Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,TMH, 2011.

2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.

3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons,2000.

4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.

5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

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M. Tech – I Year – IISem. (VLSI & Embedded Systems)

ADHOC –WIRELESS NETWORKS
(ELECTIVE -III)

UNIT -I:

Wireless LANS and PANS: Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.

AD HOC Wireless Networks: Introduction, Issues in Ad Hoc Wireless Networks.

UNIT -II:

MAC Protocols: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT -III:

Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT –IV:

Transport Layer Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT –V:

Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

TEXT BOOKS:

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.

2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.

REFERENCE BOOKS:

1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C.K. Toh , 1st Ed. Pearson Education.

2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer.

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DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(ELECTIVE -III)

UNIT –I:

Introduction to Digital Signal Processing:

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences.Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems,Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II:

Architectures for Programmable DSP Devices:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III:

Programmable Digital Signal Processors:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:

Analog Devices Family of DSP Devices:

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Blackfin Processor - The Blackfin Processor, Introduction to Micro Signal Architecture,Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V:

Interfacing Memory and I/O Peripherals to Programmable DSP Devices:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

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TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture
Publisher: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D.,California Technical Publishing, ISBN 0-9660176-3-3, 1997
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes ISBN 0750679123, 2005

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M. Tech – I Year – IISem. (VLSI & Embedded Systems)

EMBEDDED NETWORKING
(ELECTIVE -III)

UNIT –I:

Embedded Communication Protocols:

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire

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UNIT –II:

USB and CAN Bus:

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication:Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors – Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III:

Ethernet Basics:

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV:

Embedded Ethernet:

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V:

Wireless Embedded Networking:

Wireless sensor networks – Introduction – Applications – Network Topology – Localization – Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari?, Cambridge press 2005.

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M. Tech – I Year – IISem. (VLSI & Embedded Systems)

SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -IV)

UNIT –I:

Introduction to the System Approach:

System Architecture, Components of the system, Hardware & Software, Processor

UNIT –II:

Processors:

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

Simple Processor – memory interaction.

UNIT –III:

Memory Design for SOC:

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT -IV:

Interconnect Customization and Configuration:

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V:

Application Studies / Case Studies:

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2 nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1 st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.

System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L,2001, Kluwer Academic Publishers.

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DESIGN FOR TESTABILITY
(ELECTIVE -IV)

UNIT -I:
Introduction to Testing:
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:
Logic and Fault Simulation:
Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III:
Testability Measures:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and **Scan Design:** Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:
Built-In Self-Test:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation,N Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:
Boundary Scan Standard:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pi n Descriptions.

TEXT BOOKS:
1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:
1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Frieman, Jaico Publishing House
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press..

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M. Tech – I Year – IISem. (VLSI & Embedded Systems)

MULTIMEDIA AND SIGNAL CODING
(ELECTIVE-IV)

UNIT-I: Introduction to Multimedia: Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.

Color in Image and Video: Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Out-of-Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model.

UNIT-II: Video Concepts: Types of Video Signals, Analog Video, Digital Video.

Audio Concepts: Digitization of Sound, Quantization and Transmission of Audio.

UNIT-III: Compression Algorithms:

Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.

Lossy Image Compression Algorithms: Transform Coding: KLT And DCT Coding, Wavelet Based Coding.

Image Compression Standards: JPEG and JPEG2000.

UNIT-IV:

Video Compression Techniques: Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and InterFrame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT-V:

Audio, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

TEXT BOOKS:

1. Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI, 2010.
2. Multimedia Signals & Systems – Mrinal Kr. Mandal Springer International Edition 1st Edition, 2009.

REFERENCE BOOKS:

1. Multimedia Communication Systems – Techniques, Stds & Netwroks K.R. Rao, Zorans. Bojkoric, Dragorad A. Milovanovic, 1st Edition, 2002.
2. Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition, 2009.
3. Multimedia Systems John F. Koegel Bufond Pearson Education (LPE), 1st Edition, 2003.
4. Digital Video Processing – A. Murat Tekalp, PHI, 1996.

Video Processing and Communications – Yaowang, Jorn Ostermann, Ya-QinZhang, Pearson, 2002

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M. Tech – I Year – IISem. (VLSI & Embedded Systems)

NATURAL LANGUAGE PROCESSING
(OPEN ELECTIVE-I)

UNIT I

Introduction and Overview What is Natural Language Processing, hands-on demonstrations. Ambiguity and uncertainty in language. The Turing test.

Regular Expressions Chomsky hierarchy, regular languages, and their limitations. Finite-state automata. Practical regular expressions for finding and counting language phenomena. A little morphology. Exploring a large corpus with raged tools. P**rogramming in Python** An introduction to programming in Python. Variables, numbers, strings, arrays, dictionaries, conditionals, iteration. The NLTK (Natural Language Toolkit)

String Edit Distance and Alignment Key algorithmic tool: dynamic programming, a simple example, use in optimal alignment of sequences. String edit operations, edit distance, and examples of use in spelling correction, and machine translation.

UNIT II

Context Free Grammars Constituency, CFG definition, use and limitations. Chomsky Normal Form. Top-down parsing, bottom-up parsing, and the problems with each. The desirability of combining evidence from both directions

Non-probabilistic Parsing Efficient CFG parsing with CYK, another dynamic programming algorithms. Early parser. Designing a little grammar, and parsing with it on some test data.

Probability Introduction to probability theory Joint and conditional probability, marginals, independence, Bayes rule, combining evidence. Examples of applications in natural language.

Information Theory The "Shannon game"--motivated by language! Entropy, cross entropy, information gain. Its application to some language phenomena.

UNIT III

Language modeling and Naive Bayes

Probabilistic language modeling and its applications. Markov models. N-grams. Estimating the probability of a word, and smoothing. Generative models of language. Part of Speech Tagging and Hidden Markov Models**,** Viterbi Algorithm for Finding Most Likely HMM Path Dynamic programming with Hidden Markov Models, and its use for part-of-speech tagging, Chinese word segmentation, prosody, information extraction, etc.

UNIT IV

Probabilistic Context Free Grammars

Weighted context free grammars. Weighted CYK. Pruning and beam search.

Parsing with PCFGs

A tree bank and what it takes to create one. The probabilistic version of CYK. Also: How do humans parse? Experiments with eye-tracking. Modern parsers.

Maximum Entropy Classifiers

The maximum entropy principle and its relation to maximum likelihood. Maximum entropy classifiers and their application to document classification, sentence segmentation, and other language tasks

UNIT V

Maximum Entropy Markov Models & Conditional Random Fields

Part-of-speech tagging, noun-phrase segmentation and information extraction models that combine maximum entropy and finite-state machines. State-of-the-art models for NLP.

Lexical Semantics Mathematics of Multinomial and Dirichlet distributions, Dirichlet as a smoothing for multinomial's.

Information Extraction & Reference Resolution- Various methods, including HMMs. Models of anaphora resolution. Machine learning methods for co reference.

TEXT BOOKS:

1. "Speech and Language Processing": Jurafsky and Martin, Prentice Hall
2. "Statistical Natural Language Processing"- Manning and Schutze, MIT Press
3. "Natural Language Understanding". James Allen. The Benajmins/Cummings Publishing Company

REFERENCES BOOKS:

1. Cover, T. M. and J. A. Thomas: Elements of Information Theory. Wiley.
2. Charniak, E.: Statistical Language Learning. The MIT Press.
3. Jelinek, F.: Statistical Methods for Speech Recognition. The MIT Press.
4. Lutz and Ascher - "Learning Python", O'Reilly

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M. Tech – I Year – IISem. (VLSI & Embedded Systems)

ADVANCED NETWORK PROGRAMMING
(OPEN ELECTIVE-II)

UNIT – I

Linux Utilities- File handling utilities, Security by file permissions, Process utilities, Disk utilities, Networking utilities, Filters, Text processing utilities and Backup utilities. Bourne again shell(bash) - Introduction, pipes and redirection, here documents, running a shell script, the shell as a programming language, shell meta characters, file name substitution, shell variables, command substitution, shell commands, the environment, quoting, test command, control structures, arithmetic in shell, shell script examples. Review of C programming concepts-arrays, strings (library functions), pointers, function pointers, structures, unions, libraries in C.

UNIT - II

Files- File Concept, File types File System Structure, Inodes, File Attributes, file I/O in C using system calls, kernel support for files, file status information-stat family, file and record locking-lockf and fcntl functions, file permissions- chmod, fchmod, file ownership-chown, lchown , fchown, linkssoft links and hard links – symlink, link, unlink. File and Directory management – Directory contents, Scanning Directories- Directory file APIs. Process- Process concept, Kernel support for process, process attributes. Process control – process creation, replacing a process image, waiting for a process, process termination, zombie process, orphan process.

UNIT - III

Signals- Introduction to signals, Signal generation and handling, Kernel support for signals, Signal function, unreliable signals, reliable signals, kill, raise , alarm, pause, abort, sleep functions. Interprocess Communication - Introduction to IPC mechanisms, Pipes- creation, IPC between related processes using unnamed pipes, FIFOs-creation, IPC between unrelated processes using FIFOs(Named pipes), differences between unnamed and named pipes, popen and pclose library functions, Introduction to message queues, semaphores and shared memory. Message Queues- Kernel support for messages, UNIX system V APIs for messages, client/server example. Semaphores-Kernel support for semaphores, UNIX system V APIs for semaphores.

UNIT – IV

Shared Memory- Kernel support for shared memory, UNIX system V APIs for shared memory, client/server example. Network IPC - Introduction to Unix Sockets, IPC over a network, Client-Server model ,Address formats(Unix domain and Internet domain), Socket system calls for

Connection Oriented - Communication, Socket system calls for Connectionless-Communication, Example-Client/Server Programs- Single Server-Client connection, Multiple simultaneous clients, Socket options – setsockopt, getsockopt, fcntl.

UNIT-V

Network Programming in Java-Network basics, TCP sockets, UDP sockets (datagram sockets), Server programs that can handle one connection at a time and multiple connections (using multithreaded server), Remote Method Invocation (Java RMI)-Basic RMI Process, Implementation details-Client-Server Application.

TEXT BOOKS:

1. Unix System Programming using C++, T.Chan, PHI.(Units II,III,IV)
2. Unix Concepts and Applications, 4th Edition, Sumitabha Das, TMH.(Unit I)
3. An Introduction to Network Programming with Java, Jan Graba, Springer, rp 2010.(Unit V)
4. Unix Network Programming ,W.R. Stevens, PHI.(Units II,III,IV)
5. Java Network Programming,3rd edition, E.R. Harold, SPD, O'Reilly.(Unit V)

REFERENCE BOOKS:

1. Linux System Programming, Robert Love, O'Reilly, SPD.
2. Advanced Programming in the UNIX environment, 2nd Edition, W.R.Stevens, Pearson Education.
3. UNIX for programmers and users, 3rd Edition, Graham Glass, King Ables, Pearson Education.
4. Beginning Linux Programming, 4th Edition, N.Matthew, R.Stones, Wrox, Wiley India Edition.
5. Unix Network Programming The Sockets Networking API, Vol.-I,W.R.Stevens, Bill Fenner, A.M.Rudoff, Pearson Education.
6. Unix Internals, U.Vahalia, Pearson Education.
7. Unix shell Programming, S.G.Kochan and P.Wood, 3rd edition, Pearson Education.
8. C Programming Language, Kernighan and Ritchie, PHI

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M. Tech – I Year – IISem. (VLSI & Embedded Systems)

GRID AND CLOUD COMPUTING
(Elective-IV)

UNIT-I

System models for advanced computing –clusters of cooperative computing, grid computing and cloud computing; software systems for advanced computing-service oriented software and parallel and distributed programming models with introductory details, Features of grid and cloud platform.

UNIT-II

Cloud Computing services models and features in Saas, Paas and Iaas.
Service oriented architecture and web services; Features of cloud computing architectures and simple case studies.

UNIT-III

Virtualization- Characteristic features, Taxonomy Hypervisor, Virtualization and Cloud Computing, Pros and Cons of Cloud Computing, Technology Examples/Case Studies.

UNIT-IV

Cloud programming Environmental- Map Reduce Hadoop Library from Apache, Open Source Cloud Software Systems –Eucalyptus.

UNIT-V

Grid Architecture and Service modeling, Grid resource management, Grid Application trends.

TEXT BOOKS:

1. Distributed and Cloud Computing, Kaittwang Geoffrey C.Fox and Jack J Dongrra, Elsevier India 2012.
2. Mastering Cloud Computing- Raj Kumar Buyya, Christian Vecchiola and S.Tanurai Selvi, TMH, 2012.

REFERENCE BOOKS:

1. Cloud Computing, John W. Ritting House and James F Ramsome, CRC Press, 2012.
2. Enterprise Cloud Computing, Gautam Shroff, Cambridge University Press, 2012.

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EMBEDDED SYSTEMS LABORATORY

Note:
The following programs are to be implemented on ARM based Processors/Equivalent.
Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

Part -I: The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for a. Addition | Subtraction | Multiplication | Division
b. Operating Modes, System Calls and Interrupts
c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

Part -II:

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.